IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Stefan Marco Koch et al.
Application No.	:	10/521,881
Filed	:	September 28, 2005
For	:	INTER-PROCESSOR COMMUNICATION SYSTEM FOR COMMUNICATION BETWEEN PROCESSORS
Examiner	:	George Giroux
Art Unit	:	2183
Docket No.	:	853663.412USPC
Date	:	April 28, 2010

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' REPLY BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on March 26, 2009 and is in response to the Examiner's Answer mailed on March 2, 2010. Appellants hereby requests any fees necessary for acceptance of this Reply Brief be charged to Deposit Account No. 19-1090.

I. ARGUMENT IN REPLY

This reply brief primarily addresses four arguments raised in the Examiner's Answer. Where the arguments correspond to main headings in Appellants' Supplemental Brief, those headings will be used for convenience. For brevity, other than by incorporation, subheadings are not included in this reply brief. The Examiner's Answer provided other arguments/assertions, which are believed to be insufficient to meet the Examiner's burden to establish a *prima facie* case of anticipation or obviousness or to overcome Appellants' arguments

for patentability set forth in Appellants' Supplemental Brief. For the sake of brevity, these arguments set forth in Appellants' Brief will not be repeated herein.

A. *Claims 13, 14, 16, 18 and 19 Are Not Anticipated by Koch*

In view of the Examiner's entry of an amendment to claim 13 after final, the Examiner no longer contends claims 13, 14, 16, 18 and 19 are anticipated by Koch. Accordingly, the rejection of claims 13, 14, 16, 18 and 19 as anticipated by Koch should be reversed. While the Examiner appears to apologize to the Board for the inconvenience of changing the status of the rejections (see Examiner's Answer at 3, paragraph 9), Appellants believe the Examiner should be commended for narrowing the issues to be presented on appeal, and Appellants thank the Examiner for doing so.

B. *Claims 1-7, 9 and 10 Are Not Rendered Obvious by Koch in View of Tang*

Appellants incorporate the argument presented in the Supplemental Appellants' Brief on pages 6-10 and 12-14.

First, the Examiner argues Appellants may not attack the references separately when a rejection is based on a combination of the references. This is a mischaracterization of Appellants' position. Appellants instead argued that particular recited features are absent from both references, and that the Examiner had failed to present a convincing line of reasoning for the further modification. For example, with regard to claim 1, Appellants argued that neither reference discloses two programmable units, each of which has two external direct memory access channel interfaces, each on one of two clocks.

Second, the Examiner attempts to gloss over the fact that further modifications to the combination of Koch and Tang would be required to achieve the claimed embodiments by arguing that "it would be obvious, in light of the setup of Koch, that when adding the second external channel to each DMA, as taught by Tang ... that these two channels would also be on the clock domain of their respective processors." Examiner's Answer at 21. This is both an admission that a further modification to the combination of Koch and Tang is required, and a conclusory statement that the further modification would be obvious. A conclusory statement that the further modifications to the cited references are obvious is, however, insufficient to

establish a *prima facie* case of obviousness. *Ex parte Nancy C. Frye*, 94 U.S.P.Q. 2d 1072, -, 2010 WL 889747 at *5 (Bd.Pat.App. & Interf. 2010) "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.") (citations omitted).

The Examiner's only specific answer as to why this additional modification would allegedly be obvious is his conclusory and incorrect assertion that Tang would motivate coupling coupling DMA2 54 of Koch to access unit 51 of Koch. But this is not what the combination of Tang and Koch would teach. Instead, the combination would teach coupling another shareable unit 53 to the second processor system bus 50 through another DMA channel interface. Figure 9 of Tang and the description thereof demonstrate that the DMA channel interfaces of Tang to which the Examiner points are Ethernet0 Controller Interface 907, the Ethernet Controller Interface 908 and Peripheral Controller Interface 909: "Also included in the apparatus are DMA channel interfaces such as an Ethernet0 Controller Interface 907, Ethernet1 Controller Interface 908, and Peripheral Controller Interface 909." Tang, Column 7, lines 38-41 (describing Figure 9 of Tang). The Ethernet0 Controller Interface 907, Ethernet1 Controller Interface 908, and Peripheral Controller Interface 909 of Tang correspond to the shareable units 53 of Koch.

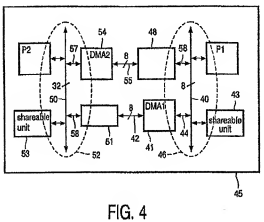

FIG. 4

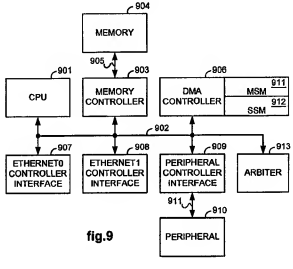

fig.9

Figure 4 of Koch and Figure 9 of Tang

For convenience, Figure 4 of Koch and Figure 9 of Tang are produced above. Thus, Tang, when combined with Koch, would suggest coupling a second shareable unit to the bus 50 through a DMA channel interface. There is nothing in Tang to suggest coupling DMA2 54 of Koch to access unit 51 of Koch through another DMA channel interface, or DMA1 to access unit 48, and nothing in the combination of Koch and Tang to suggest or otherwise render this further modification obvious. There is nothing in the "setup" of Koch to suggest this further modification. The Examiner's conclusory statement that further modification is not required is unsupported by the references or any articulated reasoning, other than that this further modification would achieve the claimed embodiment. This is classic, and improper, hindsight reasoning.

Thus, the Examiner has failed to show that Koch, alone or in combination with Tang, renders obvious "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock, wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit," as recited in claim 1. Claims 2-7, 9 and 10 depend from claim 1 and are allowable at least by virtue of their dependencies.

The Examiner also argues in the Examiner's Answer that "the claims do not explicitly require that the first and second processor clocks are different, though they have been assumed so for the sake of advancing prosecution." Examiner's Answer at 22. Claim 1 recites, "a first processor on a first clock coupled to the first processor bus; ... a second processor on a second clock coupled to the second processor bus." It is not reasonable to interpret the recited first and second clocks as the same clock in view of the claims, the specification or the prosecution history, and it does not advance prosecution to raise such an argument on appeal when Appellants consistently and expressly argued to the Examiner that the combination of the cited references did not disclose two programmable units each of which has two direct memory access channels one on each of two clocks. *See, e.g.,* Amendment of January 26, 2009 at 9; Amendment of August 14, 2008 at 10.

C. *Claims 13-19 Are Not Rendered Obvious by Koch, Alone or in Combination with Tang*

Appellants incorporate the argument presented in the Supplemental Appellants' Brief on pages 6-10 and 14-17.

To the extent the Examiner contends Appellants are attacking the references separately, as noted above the Examiner is mischaracterizing Appellants' argument. Appellants instead argued that the combination of Koch and Tang did not contain all of the recited elements and that the Examiner had not presented a convincing line of reasoning as to why one of skill in the art would have found the required further modifications obvious. For example, with regard to claim 13 Appellants argued that Koch, alone or in combination with Tang, was missing the "first bi-directional channel [comprising]: a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and ... second bi-directional channel [comprising]: a second external channel of the first DMA unit to operate on the first processor clock; and a second external channel of the second DMA unit to operate on the second processor clock." With regard to claim 14, Appellants argued the combination of Koch and Tang was also missing a first bidirectional channel comprising a first programmable unit coupled between the first external channel of a first DMA unit and the first external channel of the second DMA unit. With regard to claim 15, Appellants also argued Koch, alone or in combination with Tang, is missing "a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock."

To reject independent claim 13, the Examiner relies on the same argument presented to reject claim 1, namely that Tang suggests adding a second external DMA channel interface coupling DMA2 to access unit 51. As demonstrated above, Tang would instead suggest

coupling an additional shareable unit to bus 50 through a DMA channel interface. Thus, the Examiner has not presented a convincing line or reasoning for why one of skill in the art would have found the further modifications of the combination of Koch and Tang necessary to achieve the embodiments claimed in claims 13, 14 and 15 to be obvious. Claims 16-19 depend from claim 13 and are allowable at least by virtue of their dependency.

The Examiner argues in the Examiner's Answer that "the claims do not explicitly require that the first and second bi-directional channels not be the same bi-directional channel, or similarly with the DMA's, etc., though they have been assumed to be different for the sake of advancing prosecution." For convenience, claim 13 is set forth below.

13. A system comprising:

a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock;

a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock;

a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface to the second processor, wherein the first bi-directional channel comprises:

a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and

a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and

a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first

bi-directional channel between the first and second bus, wherein the second bi-directional channel comprises:

a second external channel of the first DMA unit to operate on the first processor clock; and

a second external channel of the second DMA unit to operate on the second processor clock.

It is not reasonable to interpret the recited "first processor and first shareable unit operating on a first processor clock" and "second processor and second shareable unit operating on a second processor clock" as a single clock, the recited "first bi-directional channel" and "second bi-directional channel" as a single bi-directional channel, or the recited "first DMA unit" and "second DMA unit" as a single DMA unit, in view of the language of claim 13, the specification or the prosecution history. It also does not advance prosecution to raise such an argument on appeal.

II. Conclusion of Argument

For at least the reasons set forth in Appellants' Supplemental Brief, and those set forth above, the Examiner has failed to meet his burden of establishing a *prima facie* case for rejecting the claims. Accordingly, Appellants respectfully submit that all of the pending claims are allowable and request that the Examiner's rejections thereof be reversed.

Respectfully submitted,
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